

CLAIMS

5 1. A receiver partially implemented on an integrated circuit chip, the receiver comprising:

means on the chip for receiving a plurality of channels of signals in a radio frequency telecast band;

a first mixer on the chip to which the television signals are applied;

10 a first bandpass filter off the chip coupled onto the chip to the output of the first mixer; the first filter having a first pass band;

a first local oscillator (LO) on the chip coupled to the first mixer, the first LO having a variable frequency;

15 means on the chip for adjusting the first LO to select one of the channels and shift the selected channel to the first pass band;

a second mixer on the chip to which the selected channel is applied after the first mixer;

20 a second LO on the chip coupled to the second mixer, the second LO having a fixed frequency that shifts the selected channel to an intermediate frequency; and

means for demodulating the selected channel.

25 2. The television receiver of claim 1, additionally comprising a second bandpass filter off the chip coupled onto the chip to the output of the second mixer; the second filter having a second pass band, the second LO having a frequency that shifts the selected channel to the second pass band.

30 3. The television receiver of claim 1, in which the receiving means, the first LO, and the second LO have differential outputs, the first and second mixers have differential inputs and outputs, and the first bandpass filter
35 has a differential input and a differential output.

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1 36232/PBH/B600 (BP 1255)

4. An integrated receiver comprising:

5 a substrate providing a physical medium upon which a
receiver circuit is disposed;
a first local oscillator;
a second local oscillator;
a mixer having its circuit elements disposed upon the
substrate for converting a received signal to a first IF using
10 the first local oscillator's output to mix the received signal
with;
a first buffer amplifier having its circuit elements
disposed upon the substrate cascaded after the mixer;
an external first differential filter assembly coupled
15 to the first buffer amplifier output for removing an image
distortion from the first IF and removing unwanted channels;
a second buffer amplifier having its circuit elements
disposed upon the substrate coupled to the external first
differential filter assembly output;
20 a first I/Q mixer disposed upon the substrate for
converting the first IF to a second IF I and Q signal and
rejecting a first IF image distortion;
a polyphase circuit for combining the second IF I and
Q signals into a second IF signal;
25 a third buffer amplifier having its circuit elements
disposed upon the substrate and cascaded with the polyphase
circuit; and
an external second differential filter assembly coupled
to the third buffer amplifier output for removing an image
30 distortion from the second IF and removing unwanted channels;
whereby frequency conversion, channel selectivity and
image rejection are performed on the integrated circuit.

5. The integrated receiver of claim 4 additionally
35 comprising an AGC circuit having its circuit elements disposed

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upon the substrate, cascaded after the external second differential filter assembly.

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6. The integrated receiver of claim 4 additionally comprising a programmable gain attenuator and LNA circuit having its circuit elements disposed upon the substrate, cascaded in front of the first mixer.

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7. The integrated receiver of claim 4 wherein the substrate is silicon.

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8. The integrated receiver of claim 4 wherein the substrate comprises devices fabricated according to standard CMOS processing.

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9. The integrated receiver of claim 4 further comprising interconnection by differential signal transmission lines.

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